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Minimum Transistor Loss Control of an Induction Heating Inverter With LLC Resonant Load

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Abstract – **Center-aligned and edge-aligned PWM control methods for a voltage-source induction heating inverter are presented. Both phase-shifted mode (PSM) and discontinuous current mode (DCM) are discussed. There are shown power control characteristics and IGBT transistor losses of the inverter with LLC resonant load. Control trajectory for transistor loss minimization is chosen. There are presented PLL and PWM control loop simulation and experimental results.**

I. INTRODUCTION

IGBT-converters supplying third order resonant tanks have attracted attention due to particularities, which recommend these tanks in some applications over the traditional serial resonant tank.

The hybrid series-parallel LLC load (Fig. 1) can be used for impedance matching at the inverter output and to adapt the inductance of the heating inductor. Besides, due to its equivalence with the serial resonant load, the term of '*Transformerless Series Resonant Inverter*' resulted [6].

The equivalent circuit is obtained by '*resonance transformation*' [2]. Inductor L_s, often called '*transformation inductor*', has several times the value of the heating coil's inductance. The current transfer ratio between the inductor current and the inverter output current can be calculated using a first order harmonics approximation.

It can be shown [3] that the maximum load power dissipation occurs approximately at resonance frequency

$$\omega_0 = \frac{1}{\sqrt{L_{eq} C_p}}; \quad (1)$$

$$L_{eq} = L_s \parallel Lp\,. \quad (2)$$

The LLC circuit can be designed so that it remains inductive in the whole range of operation frequencies [5], [7].

Thus an inherent short-circuit protection is provided, unlike in the case of the serial resonant tank, where short-circuit of the inductor increases the resonance frequency above the operation frequency.

Stray inductances (mainly due to the active or reactive matching transformers) are included in L_s series inductor, making the transformer specification less exigent.

Power regulation is possible-width modulation and their different combinations. In continuous current mode (CCM) one can rely on the first harmonic approach for load power calculation. Thus, the *h*-th harmonic of the inverter output voltage is a function of the duty factor:

$$V_{invout\_h} = \frac{V_{dc}}{\sqrt{2}h\pi}\sqrt{a_h^2 + b_h^2}\,; \quad (3)$$

$$a_h = \sin(h\delta) + \sin(h\pi - h\delta)\,; \quad (4)$$

$$b_h = 1 - \cos(h\pi) - \cos(h\delta) + \cos(h\pi - h\delta)\,. \quad (5)$$

The first harmonic results:

$$V_{invout\_1} = \frac{2V_{dc}}{\pi}\sqrt{1 - \cos\delta}\,. \quad (6)$$

The serial equivalent parameters of the LLC resonant load are:

$$R_e = \frac{R}{(1 - \omega^2 L_p C_p)^2 + (\omega R C_p)^2}; \quad (7)$$

$$X_e = \omega L_s + \frac{\omega L_p - \omega^3 L_p^2 C_p - \omega R^2 C_p}{(1 - \omega^2 L_p C_p)^2 + (\omega R C_p)^2}\,. \quad (8)$$

Thus, the load power will be:

$$P_{load} = \frac{4V_{dc}^2}{\pi^2}(1 - \cos\delta)\frac{R_e}{R_e^2 + X_e^2}\,. \quad (9)$$

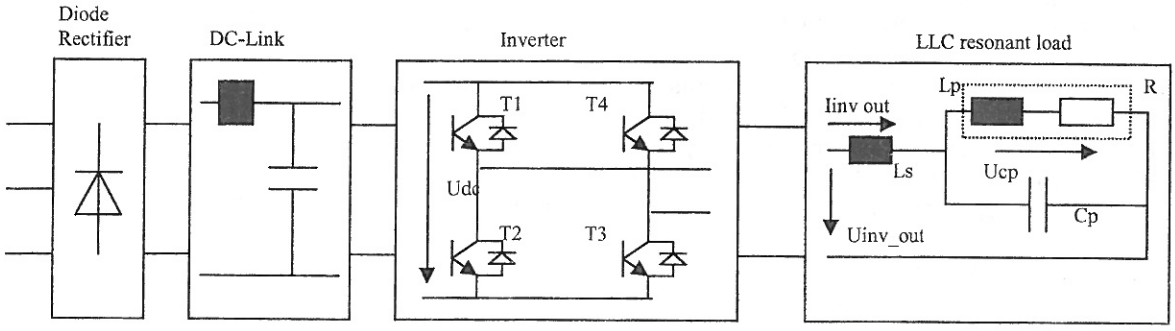

Fig.1.Structure of the converter with voltage inverter supplying a hybrid LLC resonant load

II. CONTROL METHODS

High power and high frequency operation in the range of 100 kHz is possible using IGBT-s, serial resonant tank, pulse amplitude modulation and frequency close to resonance [9]. In this case the load should be slightly inductive, operation above the resonance frequency results in lagging current and zero-voltage switching (ZVS turn-on).

However, operation with constant DC-Link voltage is desirable because of simpler and cheaper converter structure.

This can traditionally be solved by a single-input control system (either frequency or pulse width). In case of frequency-shift, the power control characteristics strongly depend on the quality factor of the inductor. Transistor losses have a maximum at average load power, leading to high thermal stress, especially at high quality factor.

In case of operation at resonance frequency and power regulation by means of pulse width modulation with voltage cancellation, the main disadvantage consists of non-zero voltage hard switching of one inverter leg, with associated diode recovery problems, making this control method improper above 10 kHz.

Generally, PLL loops are used in power and frequency control, involving combination of analog circuitry and digital programmable logic or specialized IC-s.

There are several possibilities for using combination of frequency-shift and some means of PWM, to control both power and frequency, an interaction (coupling) being present in the system.

We'll discuss PLL solutions based on the phase shift between zero transition of the capacitor tank voltage (Ucp) and a signal related to the gate signals. The later one can be aligned with the falling edge of the gate signals (referred to as '*Edge-Aligned Control*') or with the center of the time interval when both transistors of an inverter diagonal are turned on (referred to as '*Center-Aligned Control*'). The corresponding control angles are referred to as 'phi' and 'phi2' as shown in Fig. 3. Disregarding the implementation, these control methods can be assimilated either to Fig. 2 (a) or to Fig. 2 (b), which can also be found in widely spread PWM control integrated circuits.

We'll consider only control algorithms that are feasible in the presence of an active current high frequency isolation transformer, required for safety reasons.

The subject of our study is the inverter with LLC load from Fig. 1 with the following parameters:

V_{dc}=540 V, CM400HA-24H transistor model, L_s=70 µH, C_p=17.7 µF, L_p=14.13 µH, R=0.107 Ohm. Resonance frequency is close to f_0=10.9 kHz according to (1).

Fig. 3 shows the Pspice simulation waveforms resulting if the inverter legs are controlled in Phase-Shifted Mode (PSM). Gate signals of an inverter diagonal are phase-shifted against each other and angle "Phi" or "Phi2" to the zero transition of the capacitor voltage is controlled by a Phase Locked Loop.

The result is voltage cancellation due to the freewheeling intervals. The inverter legs operate in different conditions. Non-ZVS turn on can be observed in case of one leg, while hard turn off causes significant losses in the other one. Evolution of transistor losses vs. control angle 'phi2' is shown in Fig. 6 and Fig. 7 (solid curves).

Fig. 12-14 presents oscillograms in case of the same LLC load and the inverter legs controlled in "Discontinuous Current Mode (DCM)". Transistors from an inverter diagonal receive simultaneous gate pulses. After transistors are turned off, no freewheeling path exists and the inverter output current is interrupted. The inverter output voltage is not defined by the gate pulses any more, but it follows the shape of the resonant tank capacitor voltage.

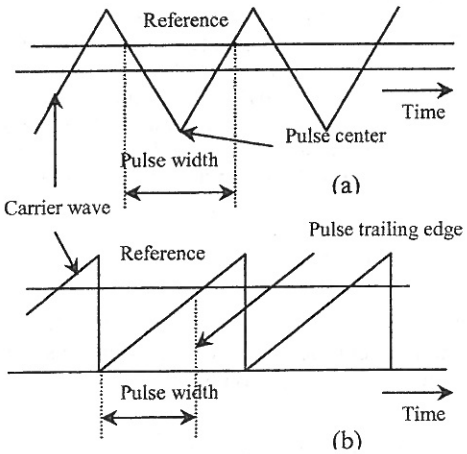

Fig.2 PW modulation control signals

The inverter legs operate in identical conditions and the transistor loss diagrams vs. 'phi2' are shown in Fig. 6 and Fig. 7 (dotted curves).

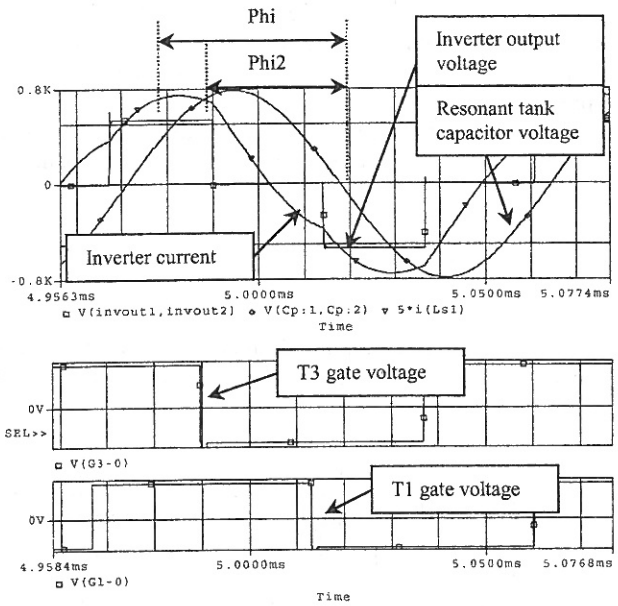

Fig.3 LLC load driven by an inverter with Phase-Shifted Mode control

Power calculation based on (9) is in good agreement with the simulation results shown in Fig. 4 and Fig. 5 (solid curves).

However, load power calculation i.e. deduction of the control characteristics is not so straightforward for the DCM inverter. Load power dependence of control angles 'phi' and 'phi2' has been obtained by PSpice simulation and represented on the same diagram with PSM characteristics in Fig. 4 and Fig. 5 (dotted curves).

It is desirable to control the inverter in a manner that results in minimum transistor losses for a given output power. Fig. 15 shows the trajectory drawn through minimum loss points belonging to different constant load power curves represented in function of duty factor and control angle.

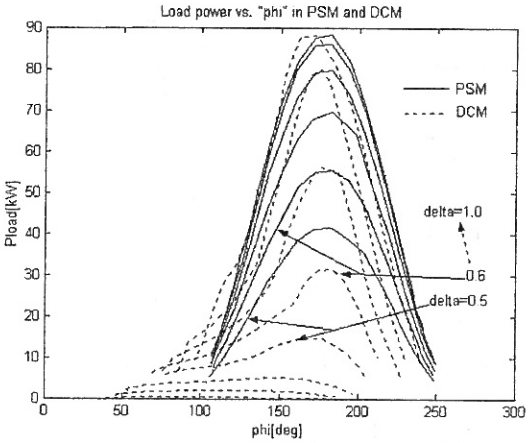

Fig.4 Load power vs. "phi" control angle in case of PSM and DCM

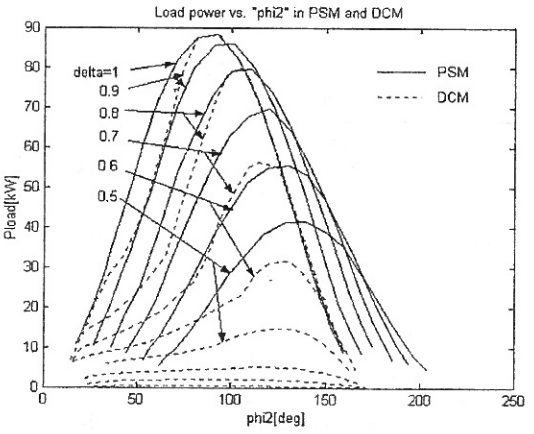

Fig.5 Load power vs. "phi2" control angle in DCM control (dotted curves) and Phase-shifted control (solid lines). The two control modes yield the same result for delta=1 duty factor.

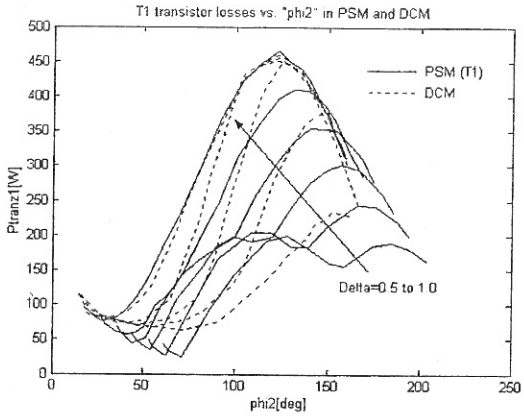

Fig.6 Transistor losses in DCM and T1 transistor losses in PSM vs. "phi2" control angle

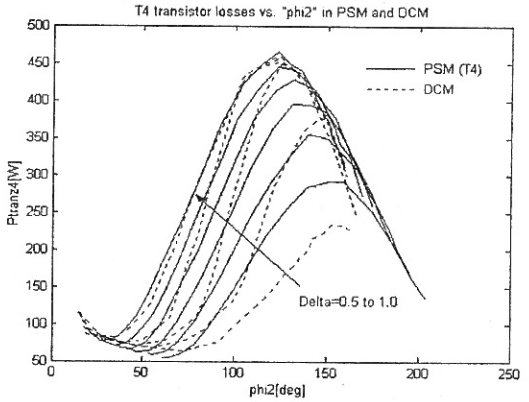

Fig.7 Transistor losses in DCM and T4 transistor losses in PSM vs. "phi2" control angle

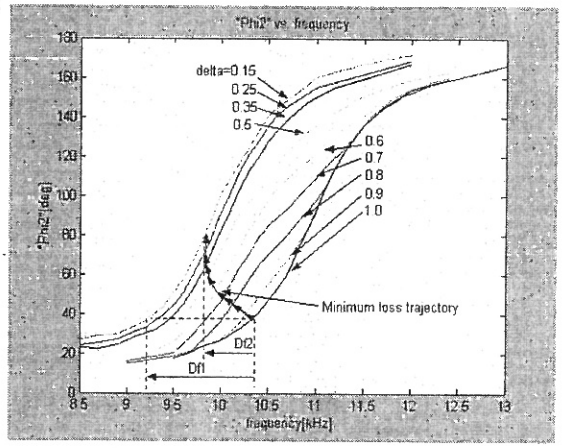

Fig.8 Df1 frequency variation in case of constant Phi2 and Df2 frequency variation in case of minimum transistor loss control

III. CONTROL SYSTEM SIMULATION

Block diagram of the Simulink control system model is presented in Fig. 11. The inverter is simulated behaviorally rather than using switches or transistor models, in order to avoid time-consuming switching detail computation.

Inverter start-up waveforms in case of constant 'Phi2' phase reference are presented in Fig. 9, start-up inverter output current and capacitor voltage being shown in detail in Fig. 10.

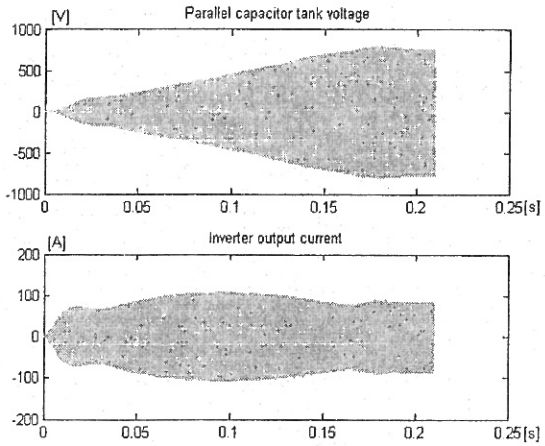

Fig.9 DCM converter startup with closed PLL and PWM control loops; several effects are simultaneously present, like ramped limitation of the PWM control voltage and the frequency regulation towards a fixed phi2=40deg

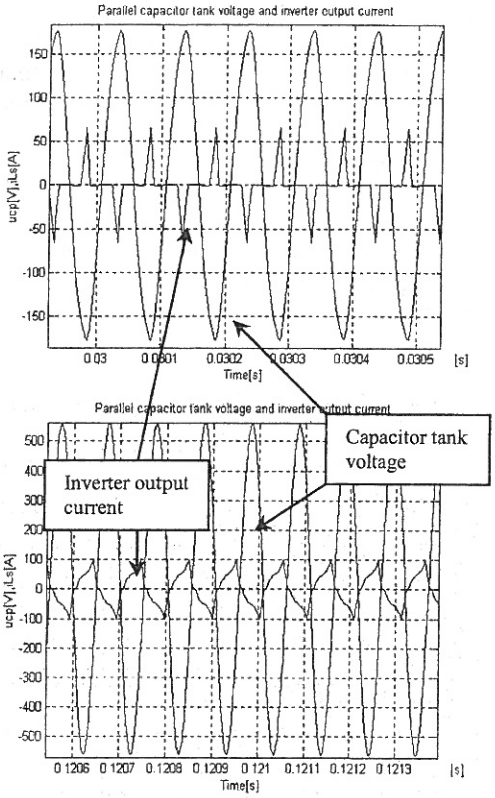

Fig.10 Capacitor voltage and inverter current in the early stages of the closed-loop start-up

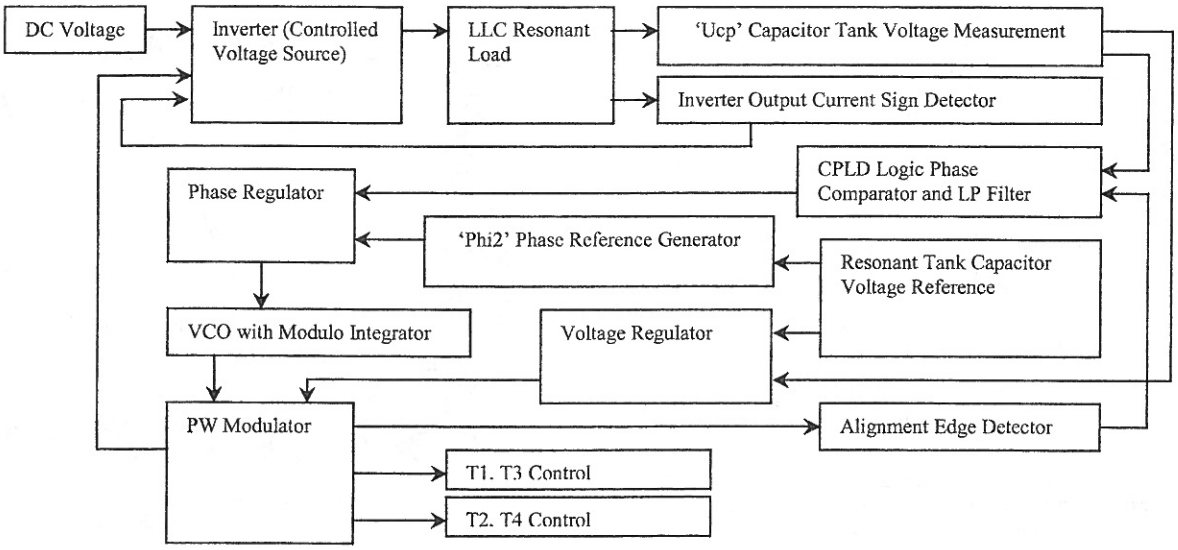

Fig.11 Block diagram of the Matlab-Simulink simulation model of the LLC resonant load capacitor tank voltage control

IV. EXPERIMENTAL RESULTS

Oscillograms of a 2 kHz, 120 kW inverter are presented in Fig.12-14. Low current turn off can be obtained when the inverter is operated according to the minimum loss control strategy. Diode recovery can be avoided in almost every operating condition.

Calorimetric transistor loss measurements proved that PSpice simulation results are sufficiently accurate for practical dimensioning purposes.

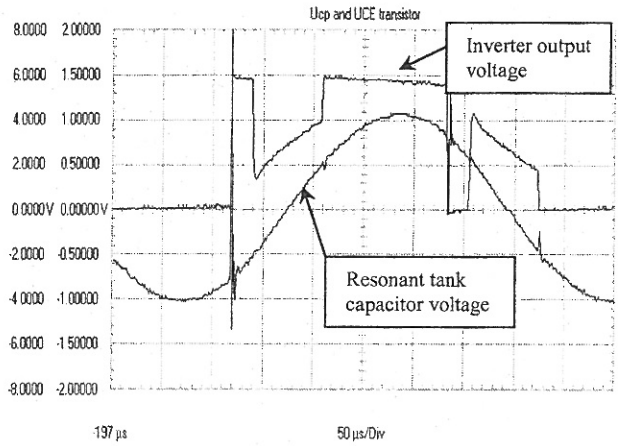

Fig.12 DCM inverter Ucp capacitor tank voltage (Ucp=880Vrms) and VCE_transistor with Pload=44kW, Vdc=550V, Idc=85A.

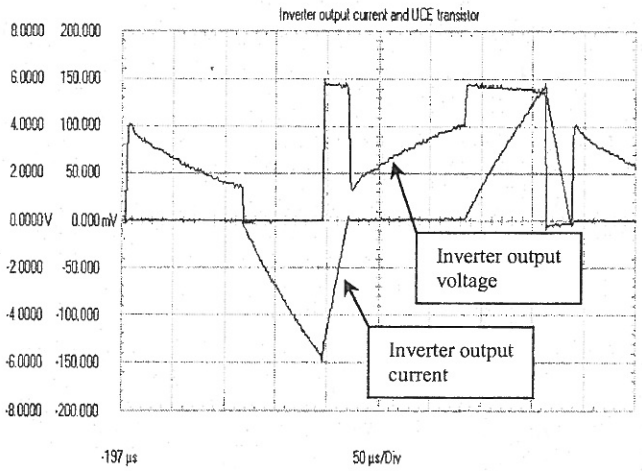

Fig.13 DCM inverter output current and UCE transistor for f=2200 Hz, Ucp=610 V, 35% duty factor

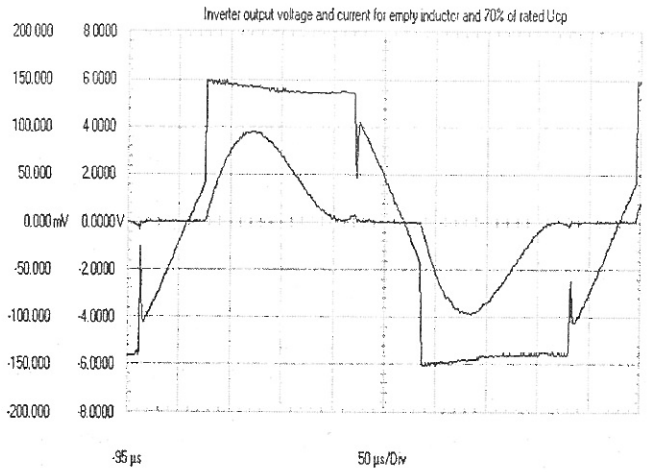

Fig.14 DCM inverter output voltage and current in case of high quality factor (empty inductor) and parallel capacitor tank voltage set to 70% of the rated value i.e. Ucp=1300 Vrms, (Pload=36 kW, fn=2 kHz)

V. CONCLUSIONS

Transistor losses have minimum values for different 'phi2' control angles, depending on the output pulse width.

Fig. 15 presents the minimum-loss power control trajectory obtained for the simulated 10 kHz converter.

This procedure will also reduce variation of operation frequency during power regulation, in comparison with frequency variation resulted for 'constant phi2 & PSM' operation (Fig. 8).

Power control characteristics become linear, easier for classical control theory application (Fig. 16).

Whereas more difficult to implement, in case of center-aligned control, a constant control angle can be defined for minimum transistor loss power control (Fig. 17).

Edge-aligned control can be a convenient solution, which makes possible the use of wide spread PWM circuits based on this technique.

The Matlab-Simulink model is suitable for long-term simulation of the converter's behavior, including start-up, steady state and short-circuit condition.

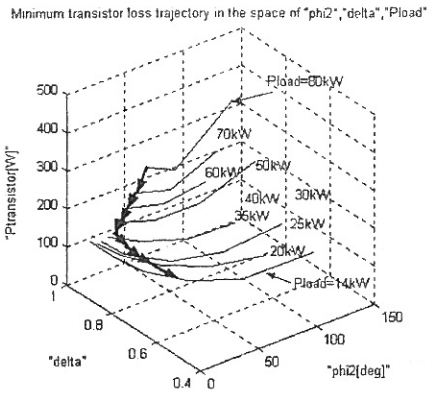

Fig.15 Minimum transistor loss trajectory in the space of 'phi2', duty factor and load power

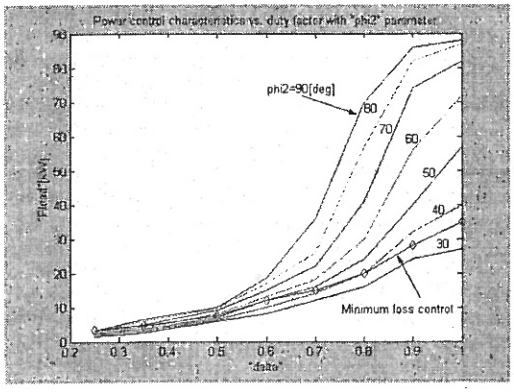

Fig.16 Load power controlled via duty factor, for constant "phi2" values and the minimum transistor loss control characteristic

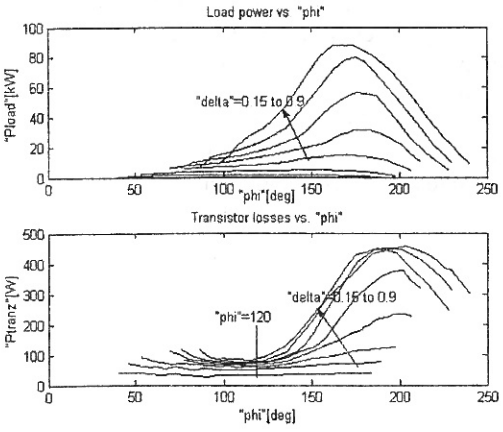

Fig.17 Load power and transistor losses vs. "phi" center-aligned control angle in DCM

VI. REFERENCES

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