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Single-Phase Current Source Induction Heater with Improved Efficiency and Package Size

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Single-Phase Current Source Induction Heater with Improved Efficiency and Package Size

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Abstract

This paper presents a modified Current Source Parallel Resonant Push-pull Inverter (CSPRPI) for single phase induction heating applications. One of the most important problems associated with current source parallel resonant inverters is achieving ZVS in transient intervals. This paper shows that a CSPRPI with the integral cycle control method has dynamic ZVS. According to this method, it is the Phase Locked Loop (PLL) circuit that tracks the switching frequency. The advantages of this technique are a higher efficiency, a smaller package size and a low EMI in comparison with similar topologies. Additionally, the proposed modification results in a low THD of the ac-line current. It has been measured as less than %2. To show the validity of the proposed method, a laboratory prototype is implemented with an operating frequency of 80 kHz and an output power of 400 W. The experimental results confirm the validity of the proposed single phase induction heating system.

Key words: Induction Heating Systems, Phase Locked Loop (PLL), Dynamic ZVS, Resonant Inverter

I. INTRODUCTION

Induction heating is a non-contact heating technique to produce very high temperatures. In each application, an appropriate frequency must be used depending on the work piece geometry and skin-depth requirements. Induction heating (IH) has been a part of high-power applications and is widely used in the industrial, office automation and electric home appliance fields. In all of these cases, there is an important need for optimal design and reduction in EMI especially for office and home appliances, which make noise on TV and radio frequency bandwidths. As a result, IH systems should be based on resonant converters to reduce the EMI effects [1]-[10]. However, with the increasing application of Induction Heating (IH) systems in various fields, concerns about the harmonic effects and power quality of the power grid have been involved in the problems facing network operation engineers.

A large number of topologies have been developed in this area, among them current-fed and voltage-fed inverters are the most commonly used [1]-[10]. An important advantage of voltage source inverters is the various control methods, such as Pulse Frequency Modulation (PFM) and Pulse Amplitude Modulation (PAM), used to control their output power [8]. However, voltage source inverters suffer from a pulsating input current. Short-circuit behavior at the resonance frequency is another disadvantage of voltage source series resonant inverters such as the class DE topology. As a result, the switching frequency must be set at a higher value [9]. The Current Source Inverter (CSI) has a limited number of control methods, but it is less affected by input voltage ripples and has short-circuited protection capability [1]-[6].

ZVS is critical for reliable operation of standard current-fed parallel resonant inverters. Under steady-state conditions, ZVS can be achieved by using common techniques such as a PLL or other integral controllers [1]. However, under transient intervals, ZVS cannot be achieved by using conventional methods. Therefore, in some current-fed parallel resonant inverters where the parallel resonant tank connects directly to the inverter, series-connected diodes are required to prevent the internal body diode of the switches from conducting [1]-[6]. Nevertheless, these diodes increase conduction losses.

In this paper, a PLL circuit is implemented based on the charge-pump phase or frequency detector. This method has poor dynamics but it possesses the phase-error elimination property at the steady state [11]. Therefore, to achieve dynamic ZVS, the input voltage must have a low slew rate at the start-up

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process [1]. The input voltage of the resonant inverter is a rectified sinusoidal wave which was presented in previous work [6]. It behaves like a ramp signal with a low slew rate near the zero crossing points. Hence the PLL is able to trace the resonant frequency at transient intervals.

In the presented study, the authors focused on dynamic ZVS and the mathematical models of the inverter parameters such as the coil design and the dc-link inductor design. It is shown that the EMI will be reduced by achieving dynamic ZVS and by removing the series-connected diodes (blocking diodes). This will be explained in greater detail in section II.

This paper presents a simple method for improving the power quality of a single phase induction heating system. The control method applied in this work is the integral cycle control. This method was also used in [12] for half-bridge voltage-source resonant inverters, and the benefits and drawbacks of this method are pointed out.

The proposed single phase induction heating is suitable for 110 VAC with 50/60Hz, because the low input impedance characteristic of the push-pull inverter allows the accessing of a power rating above 1kW for such ac-line voltage levels and high *Q*-factor induction heating applications.

II. PRINCIPLE OF OPERATION

Fig. 1 shows two conventional current mode parallel resonant inverters using only two switches in series with blocking diodes. Unlike these conventional topologies, by achieving dynamic ZVS, the two switches do not need these two blocking diodes. In this work, although both of the topologies, (a) and (b), can be implemented, it is preferable to use (b) for dc-dc converters and (a) for induction heating applications or dc-ac converters because of symmetrical current injection [2], [3]. The proposed topology is a parallel resonant push-pull inverter (a), as can be seen in Fig.1. The inductance of $L_{1,2}$ is much larger than that of the resonant inductor L_r, so under normal steady-state operation the dc-link current is approximately constant and the switching network injects an alternating square-wave current into the resonant tank [2-6]. In this circuit the two switches are operating with a duty cycle that is slightly more than half ($D > 0.5$) to achieve soft switching and to prevent the internal body diode of the power MOSFETs from conducting [6]. The inverter circuit's turn-off angle β is close to zero ($\beta \approx 0$) because the inverter is working at zero voltage and zero current switching (ZVZCS).

For the push-pull circuit, the current of L_2 which is in series with S2 is injected into the parallel resonant tank, and then returned to the dc-link when S1 is on, $0<t<T/2$. This process is repeated for S2 during the second half period, $T/2<t<T$ while the peak current of each switch is the dc-link current I_d.

At the resonant switching frequency, the voltage between diodes' anode and the power MOSFETs' source is like a half sine wave. The current of each switch is like a square wave.

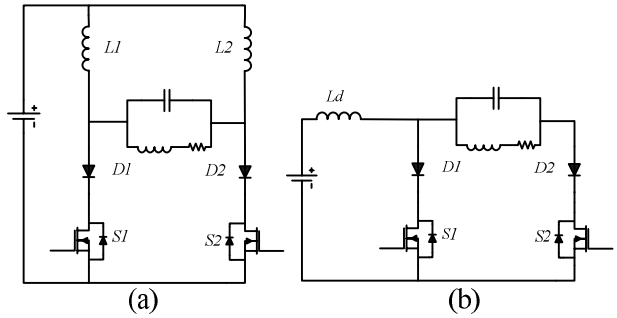

Fig. 1. The two conventional parallel resonant inverters with two switches.

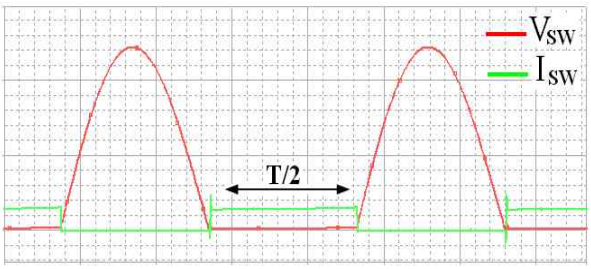

Fig. 2. The current and voltage waveforms of S_1 and S_2 without blocking diodes.

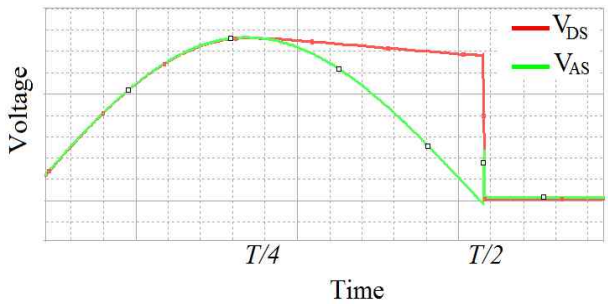

Fig. 3. Drain-to-source and anod-to-source voltages.

Fig. 2 shows the current and voltage waveform patterns of S1 and S2 when the inverter works at ZVZCS. When these two series blocking diodes (D_1 and D_2) are added in series with S1 and S2, the wave form which is shown in Fig. 2, is the voltage between the blocking diode's anode and the source of the power MOSFET. However, the voltage of the power MOSFETs will be like the wave form shown in Fig. 3. The series connected diodes (D_1 and D_2) clamp the output capacitor of the power MOSFETs to the peak voltage of the resonant tank. According to this condition, the dv/dt of the switch's voltage is too high, which causes high EMI. The remaining electric charge will be discharged when the switch turns on.

Fig. 4 shows a single phase CSPRPI without blocking diodes. A phase locked loop (PLL) circuit tracks the frequency of the soft switching under load parameter variations. The transfer function of the parallel resonant tank's impedance is derived by equation (1). By assigning a zero value to the phase of *z(s)*, the frequency at which ZVZCS occurs can be derived by equation (2).

$$Z(s) = \frac{L_r s + R}{L_r C_r s^2 + R C_r s + 1} \quad (1)$$

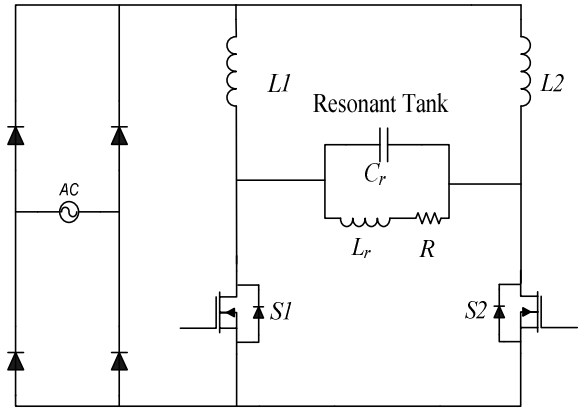

Fig. 4. The proposed CSPRPI without series connected diodes.

$$\angle Z(j\omega_{in}) = 0 \Rightarrow \tan^{-1}(\frac{\omega}{2\xi\omega_n}) - \tan^{-1}(\frac{2\xi\omega_n\omega}{\omega_n^2 - \omega^2}) = 0$$

$$\xi = \sqrt{\frac{R^2C_r}{4L_r}} \text{ and } \omega_n = \frac{1}{\sqrt{L_rC_r}} \quad (2)$$

$$\Rightarrow \omega_r = \omega_n\sqrt{1-4\zeta^2}$$

Where R, L_r, C_r, ω_n and ω_r are the load resistance, the resonant inductance, the resonant capacitance, the natural frequency of the resonant tank and the resonant frequency, respectively. R is the sum of the coil resistance and the work-piece resistance referred to the primary or coil. Another important parameter that can be defined for a parallel resonant tank is the quality factor Q which is derived by equation (3):

$$Q = \frac{\omega_r L_r}{R} \quad (3)$$

According to [2] and [6], the inverter and the resonant tank can be modeled as the RLC load shown in Fig. 5 and the parameters of the proposed modeling are derived by equation (4). Comparing the push-pull topology with the full bridge scheme, R_{eq} in the full bridge is four times that of the push-pull topology for the same resonant tank [3], [4], and [6].

$$L_{eq} = \frac{L_{1,2}}{2},\ R_{eq} = \frac{2}{\pi^2}(1+Q^2)R,\ C_{eq} = \pi^2 C_r \quad (4)$$

By assigning zero to the integral of the dc-link inductance voltage V_L over one switching period, the output voltage V_O (peak value) to the dc-link voltage V_{in} ratio K_V can be derived by equation (5):

$$\int_0^{2\pi} V_L d\theta = \int_0^{\pi} V_{in} d\theta + \int_{\pi}^{2\pi} (V_{in} - V_o \sin\theta) d\theta = 0$$

$$\hat{V}_o = \pi V_{in} \Rightarrow K_V = \pi \quad (5)$$

In order to calculate the current ripple of the dc-link, the current is considered for a half period of the switching frequency. For the second half of the switching period, the dc-link current wave form is repetitive which means that the ripple frequency of the dc-link current is twice the switching frequency. Accordingly, equation (6) formulates the dc-link current as a function of time i_d for $0<t<T$ where I_0 is the initial condition.

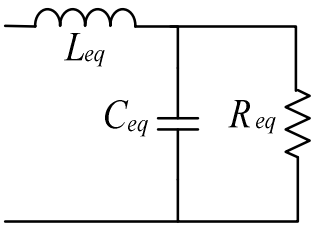

Fig. 5. The average model of resonant inverter.

$$i_d(t) = \int_0^t \frac{V_{in}}{L} dt' + \int_0^t \frac{(V_{in} - V_0)}{L} dt' + I_0 \quad (6)$$

Therefore, the current ripple Δi_d (peak to peak) of the dc-link is derived as follows:

$$\Delta i_d(t) = \int_0^t \frac{V_{in}}{L} dt' + \int_0^t \frac{V_{in}(1 - K_V Sin(\omega_r t'))}{L} dt'$$

$$\frac{\partial \Delta i_d(t)}{\partial t} = 0 \Rightarrow t_{\max} = \frac{\sin^{-1}(\frac{2}{K_V})}{\omega_r}$$

The ripple value is finally derived by equation (7). This equation shows the relationship between the dc-link inductances, the operating frequency and the dc-link ripple. By (7), the parameters of the inverter can be designed for specific data.

$$\Delta I_{dc} \cong \frac{1.152 V_{in}}{2L_{1,2}\omega_r} \quad (7)$$

The current ripple of each inductance can be derived by equation (8). In this equation, the peak-peak current of $L_{1,2}$ is attained by considering the integral voltage of each inductor over a half period when the inductance is charging. As can be seen from equations (7) and (8) the current ripple of each inductor is about 2.7 times the dc-link current ripple.

$$\Delta I_{L1,2} \cong \frac{\pi V_{in}}{L_{1,2}\omega_r} \quad (8)$$

III. Control Method

In this paper, the output current is controlled by the integral cycle control method which is a conventional method that has been used for thermal processes for the past several years [12]. Based on this control method, D_{power} is defined as the ratio of the ON state cycles to the total working cycles, and the output power of the IH at a specific D_{power} is derived from equation (10):

$$D_{power} = \frac{T_{on}}{T_{on} + T_{off}} = \frac{N}{N+M} \quad (9)$$

$$P_{out} = \frac{V_{in}^2}{2R_{eq}} D_{power} \quad (10)$$

According to equation (9), N is the number of ON cycles and M is the number of OFF cycles. The Micro Controller Unit MCU cancels some of the cycles by stopping the trigger signals of the switches at the zero crossing points, while counting the number of sine wave cycles using a zero crossing detector.

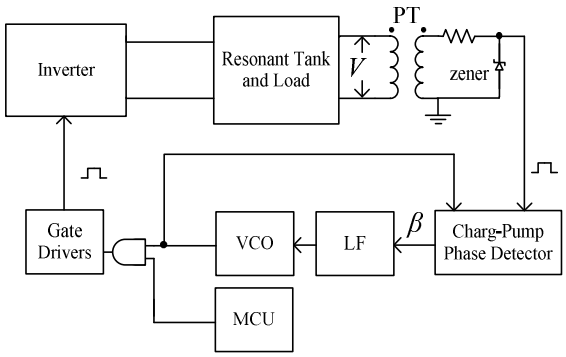

Fig. 6. Block diagram of PLL circuit, inverter and controller.

By assigning high values to the total cycles (M+N>10), the amplitude of the sub-harmonics will be negligible [13]. In the presented work, there is no dc-link capacitor, so the output current of the coil is analogous to two sinusoidal signals multiplied by each other. ω_r and ω_{in} are the resonant frequency and the ac-line frequency, respectively:

$$I_o \approx \frac{\pi\sqrt{2}V_{in}}{\omega_r L_r} Sin(\omega_{in}t)Sin(\omega_r t) \ for \ Q >> 1 \qquad (11)$$

IV. PLL Circuit

Schematics of the triggering circuits and the applied control method are shown in Fig.6. According to this figure, the transient interval of the circuit must be very fast in comparison to the ac-line period. This condition is achieved with high frequency induction heating systems (f_r > 20 kHz). For medium frequency applications, the dc-link inductances and the resonant capacitor must be designed to minimize transient distortions. In section V these parameters are designed in more detail.

In this circuit, the PLL has one sensor that senses the output voltage and it will be done by a Potential Transformer (PT). As can be seen from the principle of the operation section, the triggering signal will be in phase with the injected current in the resonant tank. Therefore, by comprising the output voltage and the instant triggering signal, the phase error will be produced. To do the comprising process, the output voltage must be rectified in half wave mode and then passed through a chopper circuit to shape the output voltage to a square wave with a 50% duty cycle. The proposed PLL circuit with the PT and the triggering circuits are shown in Fig.6. In this paper to construct the PLL circuit, an HC/HCT4046A Integrated Circuit (IC) is used.

The PLL circuit consists of a Voltage Controlled Oscillator (VCO), a Loop Filter (LF) and a Charge-Pump Phase/Frequency Detector (CP-PFD) to suppress the steady state phase error. The important parameters of the PLL circuit are the pump voltage V_p, the LF's resistor and capacitor, the center frequency f_c and the gain of the VCO unit, K_{VCO} [11].

At start-up, the duration the resonant frequency of the tank circuit will differ according to the work piece size and its magnetic characteristics. Therefore, the PLL will spend a transient duration at the zero crossing intervals to reach the resonant frequency of the load. In this condition the charge-pump circuit is charging the capacitor of the loop filter. The processes of charging and discharging the loop filter's capacitor are nonlinear and depend on the resonant tank parameters and the charge-pump circuit [11]. However, in this paper the input voltage has a low slew rate and helps the PLL to track the resonant frequency at the start-up or zero crossing intervals.

V. Resonant Tank and DC-link Inductor Designs

A. Resonant Tank

The aim of this section is to design the resonant tank and dc-link inductors for a specific rating power. For a specific parallel resonant tank, the output power can be derived by equation (12). P_{out} is the sum of the coil power loss and the work-piece power where V_{in} is the ac-line input voltage (in rms).

$$P_{out} = P_{coil} + P_{workpiece} = \frac{\pi^2 V_{in}^2}{Q_{fl}}\sqrt{\frac{C_r}{L_r}} \qquad (12)$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \Rightarrow L_r = \frac{\pi V_{in}^2}{2 f_r Q_{fl} P_{out}} \qquad (13)$$

For a fixed resonant frequency f_r, the resonant inductance will be defined in equation (13) where the Q_{fl} is the quality factor of the parallel resonant tank at nominal work-piece. This value depends on the work-piece geometry, the resistivity and the magnetic permeability. In this paper it is assumed that the full load quality factor is about 12 which is a reasonable value for hardening applications. In this paper the input ac-line voltage is about 50V (rms) and the operating frequency is about 80 kHz while the maximum power is about 400 W when the D_{power} is unit. Therefore, the resonant inductance and the resonant capacitance will be achieved at 10.5μH and 330nF, respectively. The resonant capacitor is constructed by 28 capacitors with series-parallel connections, and each capacitor is 47nF.

To design the physical parameters of a helical resonant inductor there are three important parameters: the radius, the length and the number of turns. The inductance of a helical coil can be derived by equation (14) [14]. According to equation (15), r, N, and h are the radius, the number of turns and the height of the helical coil, respectively. The helical coil is made up of copper tube with a radius of 4mm and a thickness of 0.3mm due to the skin effect. The expected value of the helix's pitch is about 1.5mm. Therefore, the total length l of the copper tube is derived by equation (15) and the height of the helix can be derived by equation (16).

$$L_r \approx \frac{10\pi\mu_0 r^2 N^2}{9r + 10h} \qquad (14)$$

$$l = 2\pi r N \qquad (15)$$

$$h = (\delta + 2r)N \qquad (16)$$

δ is the helix's pitch. According to (14)-(16) and by assigning 10.5μH to L_r, and h=100mm to the radius of the helical coil, the number of turns are about 40mm and 15turns, respectively. According to equation (13) the net efficiency of the resonant tank is derived by equation (18), where Q_{nl} and Q_{fl} are the quality factor of resonant tank at the no-load and full-load conditions, respectively.

$$\eta_{Coil} \approx 1 - \frac{Q_{fl}}{Q_{nl}} \quad for\ Q_{fl}, Q_{nl} >> 1 \tag{17}$$

B. DC-link Inductors

The designing procedure for the dc-link inductors is based on a reduction in ac-line distortions. According to equation (7) and assuming that the dc-link current ripple is less than 2%, the dc-link inductance of $L_{1,2}$ is derived by (18). In equation (18), R_{eq} is at the nominal power rating or 400 W.

$$\frac{1.152\sqrt{2}V_{in}}{L_{1,2}\omega_r} < 0.02(\frac{\sqrt{2}V_{in}}{R_{eq}}) \Rightarrow \frac{1.152R_{eq}}{0.02\omega_r} < L_{1,2} \tag{18}$$

However, the ac-line current has distortion at the zero crossing intervals for the full load condition. This condition occurs when the time constant of the RLC circuit, shown in Fig. 5, has significant values in comparison to the ac-line period. For the full load condition, the RLC model can be reduced to an R-L circuit because the time constant of the parallel R-C (R_{eq} and C_{eq}) is negligible for the full load condition.

For the full load condition, the RLC model can be reduced to an R-L circuit because the time constant of the parallel R-C (R_{eq} and C_{eq}) is negligible for the full load condition. As a result, the dc-link current of the inverter, according to the R-L model, is derived as follows:

$$i_d(t) = \frac{\sqrt{2}V_{in}}{|Z|}[s\text{in}(\omega_{in}t - \theta) + \exp(-\frac{R_{eq}t}{L_{eq}})\sin(\theta)] \tag{19}$$

$$Z = \sqrt{R_{eq}^2 + (\omega_{in}L_{eq})^2} \quad \theta = \tan^{-1}(\frac{L_{eq}\omega_{in}}{R_{eq}}) \tag{20}$$

Fig. 7 shows the ac-line THD according to the R-L load-angle θ. Fig. 8 shows the ac-line current when the R-L load-angle is 5^0 and the THD is about 3%. According to Fig. 7, the dc-link inductance is derived as follows when the THD is considered to be less than 2%.

$$\tan^{-1}(\frac{\omega_{in}L_{eq}}{R_{eq}}) < 2.5^0 \Rightarrow L_{1,2} < 2 \times 1.39 \times 10^{-4} R_{eq} \tag{21}$$

VI. Experimental Results

To investigate the proposed push-pull resonant inverter, a laboratory prototype was built and tested. The control method was implemented based on an Atmega-8 MCU and a zero crossing detector unit. The voltage and current stresses of the S1 and S2 are derived as follows:

$$V_{\max} = \pi\sqrt{2}V_{in} = \pi\sqrt{2} \times 50 \approx 222\ (V)$$

$$I_{\max} = \frac{\sqrt{2}P_{out}}{V_{in}} = \frac{\sqrt{2} \times 400}{50} \approx 11.3\ (A)$$

TABLE I
Inverter Specifications

S1,2	IRFP460
L1,2	300 μH
L_r	10.5 μH
C_r	330 nF (MKP type)
Q_{nl}	85
Q_{fl}	12
MOSFET gate driver	ICL7667

TABLE II
PLL Specifications

f_{center}	80 kHz
Loop Filter's resistor	2.2 kΩ
Loop Filter's capacitor	20 nF
Pump voltage	15 V
K_{VCO}	2000 volt/Hz

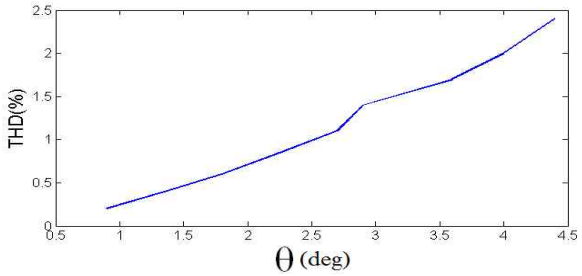

Fig. 7. Ac-line THD versus R-L load angle θ.

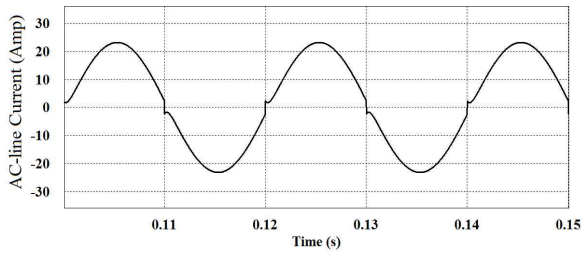

Fig. 8. Ac-line current of the single phase IH when the dc-link inductors are designed improperly.

The dc-link inductance at an operating frequency of 80 kHz and an input power of about 400 W are placed in the following range according to (18)-(21).

$$285\mu H < L_{1,2} < 3750\mu H \Rightarrow L_{1,2} \approx 300\mu H$$

The operating frequency of the proposed IH is about 80 kHz and the nominal input voltage is about 50 V (rms). The parameters of this prototype are listed in Tables I and II.

In this paper to increase the dynamic behavior of the PLL circuit, the VCO gain is designed to be high enough. However, a higher VCO gain will cause a higher sensitivity to noise. The two power MOSFETs are IRFP460 and this model has a low resistance in R_{on} (typically 0.27Ω). By considering the inductors' losses, the net efficiency of the inverter is close to 93% (conversion efficiency), while the net efficiency of the coil is derived from equation (17) as follows.

$$\eta_{Coil} = 100 \times (1 - \frac{12}{85}) \approx \%85.9$$

$$\Rightarrow \eta_{tot} = \eta_{Coil} \times \eta_{inv} \approx \%80$$

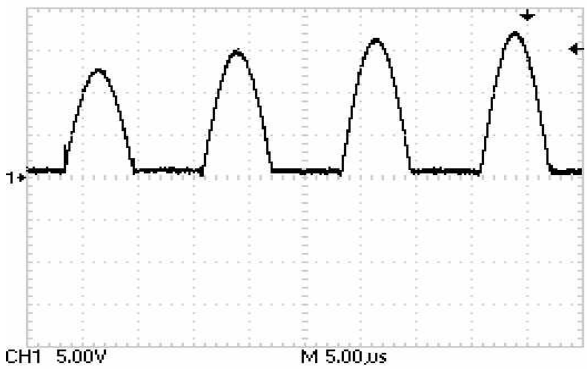

Fig. 9. Voltage of the switches at zero crossing intervals.

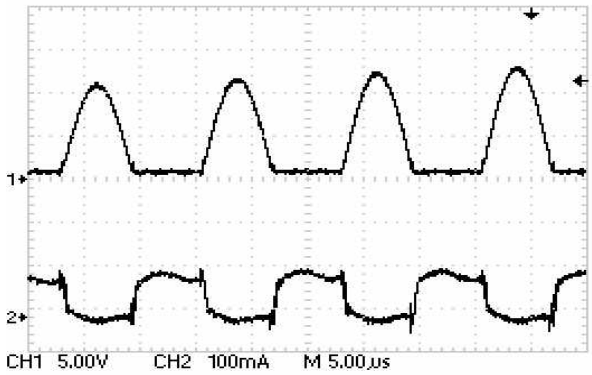

Fig. 10. Dynamic ZVZCS at zero crossing intervals.

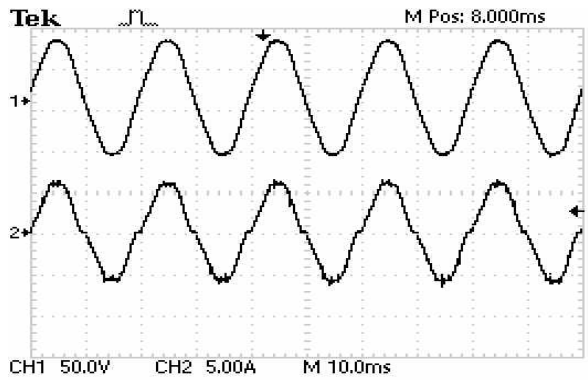

Fig. 11. Current and voltage of ac-line in full load condition.

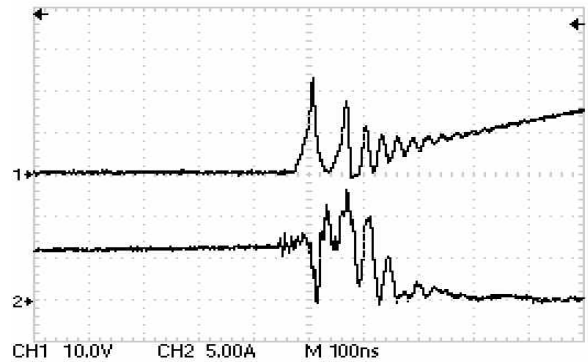

Fig. 12. Soft switching of S1 in turn-off condition.

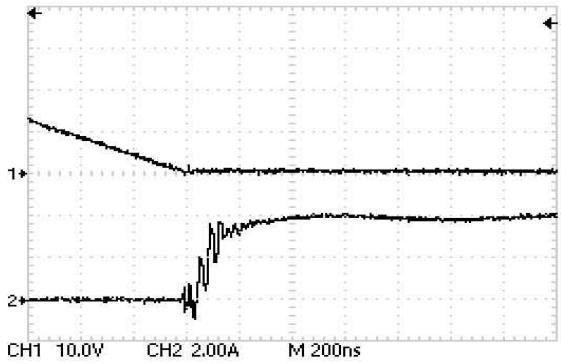

Fig. 13. Soft switching of S1 in turn-on condition.

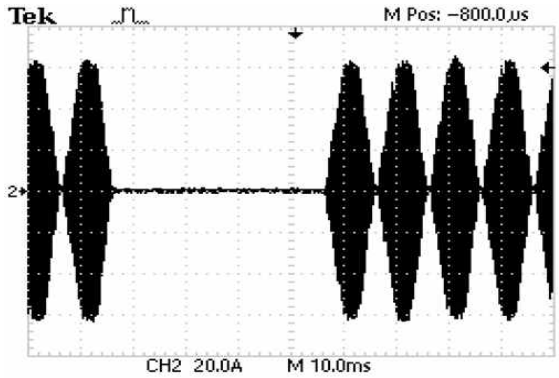

Fig. 14. Output current of the inverter when the D_{power} of 0.8.

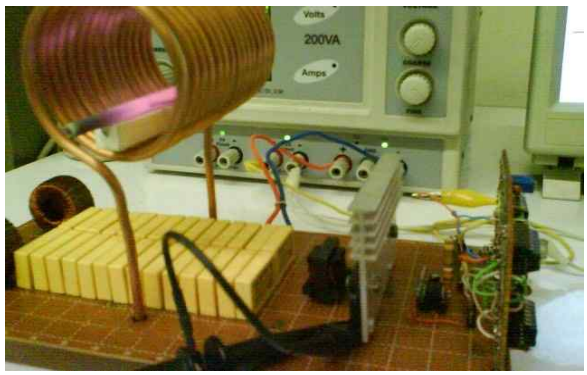

Fig .15. Laboratory prototype with PLL circuits.

In Fig.11, the ac-line voltage and current waveforms are illustrated near the full-load condition. Fig. 12 and Fig. 13 show the ZVZCS at turn off and turn on conditions in more detail.

Fig. 14 shows the output current (the coil's current) when D_{power} is equal to 0.8. The laboratory prototype with PLL circuits is shown in Fig. 15 with a work-piece.

VII. CONCLUSIONS

A modified CPRPI for single phase induction heating applications with dynamic ZVS was investigated to reduce EMI and package size. In this topology the Switch Utilization Ratio (SUR) of the switches is reduced. However, the THD of the ac-line current will be reduced significantly without adding

any additional elements. This will be a good trade-off between THD reduction and reduction of the SUR. The proposed CSPRPI is cost-effective for medium and low power IH applications. The two blocking diodes are omitted by achieving dynamic ZVS. Hence the EMI and the net efficiency of the inverter were improved.

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